

# Industrial 25G SFP28 LR 10km Optical Transceiver CLR-SFP28-LRT

## Features

- Hot-pluggable SFP28 form factor
- Full-duplex transceiver module
- 1310nm DFB laser and PIN photo-detector
- Internal CDR on both transmitter and receiver channels
- Compliant with SFP28 MSA and IEEE 802.3by 25GBASE-LR
- Compliant with CPRI/eCPRI specifications
- Data rate up to 25.78125Gbps
- Reach up to 10km over SMF
- Power consumption < 1.2W
- Dual LC receptacles
- Operating case temperature range from -40°C to +85°C
- 3.3V power supply voltage
- RoHS compliant (lead free)

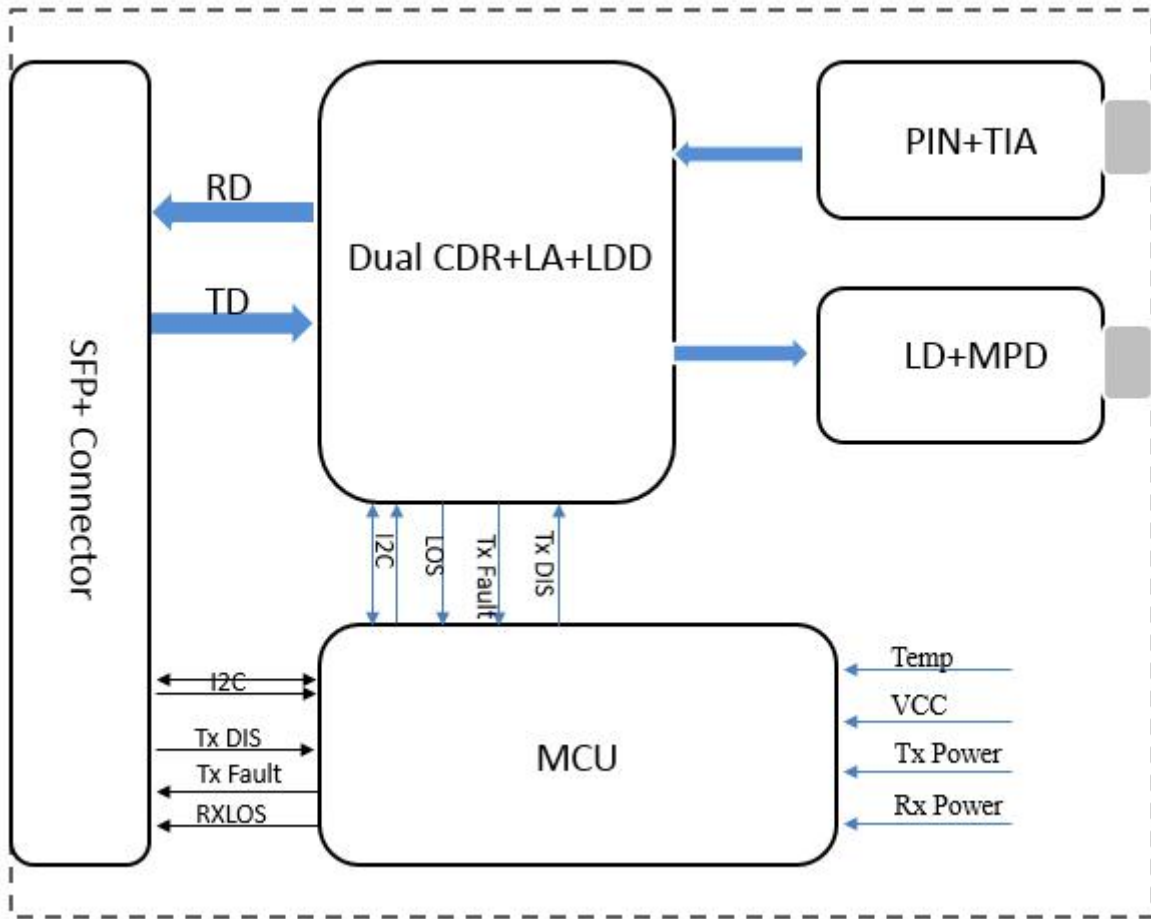


## Applications

- 25GBASE-LR Ethernet Data Center Networks
- CPRI/eCPRI 5G Fronthaul Networks

## Description

CLR Networks Industrial 25G SFP28 LR 10km Optical Transceiver CLR-SFP28-LRT is designed for Data Center 25GBASE-LR Ethernet and 5G Fronthaul CPRI/eCPRI links reach up to 10km over Single-Mode Fiber (SMF), using a nominal wavelength of 1310nm. The electrical interface uses a 20 contact edge type connector. The optical interface uses duplex LC receptacle. This module incorporates CLR Networks oven circuit and technology to provide reliable long life, high performance, and consistent service.



**Block Diagram**

### Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	0	3.6	V
Storage Temperature	Ts	-40	+85	°C
Operating Humidity	-	5	85	%

### Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	Tc	-40		+85	°C
Power Supply Voltage	Vcc	3.13	3.3	3.47	V
Power Supply Current	Icc			363	mA

## Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential Input Impedance	Zin	90	100	110	ohm
Differential Output Impedance	Zout	90	100	110	ohm
Differential Input Voltage Amplitude <sup>1</sup>	$\Delta V_{in}$	300		1100	mVp-p
Differential Output Voltage Amplitude <sup>2</sup>	$\Delta V_{out}$	500		800	mVp-p
Input Logic Level High	V <sub>IH</sub>	2.0		V <sub>CC</sub>	V
Input Logic Level Low	V <sub>IL</sub>	0		0.8	V
Output Logic Level High	V <sub>OH</sub>	V <sub>CC</sub> -0.5		V <sub>CC</sub>	V
Output Logic Level Low	V <sub>OL</sub>	0		0.4	V

### Notes:

1. Differential input voltage amplitude is measured between TxnP and TxnN.
2. Differential output voltage amplitude is measured between RxnP and RxnN.

## Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
<b>Transmitter</b>						
Data rate	BR		25.78		Gbps	
Center Wavelength	$\lambda_c$	1295	1310	1325	nm	
Spectral Width (-20dB)	$\sigma$			1	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Average Output Power	P <sub>avg</sub>	-7		3	dBm	
Optical Modulation Amplitude	OMA	-4		3	dBm	
Extinction Ratio	ER	3			dB	
Eye Mask Coordinates		{0.31, 0.4, 0.45, 0.34, 0.38, 0.4}				
<b>Receiver</b>						
Data rate	BR		25.78		Gbps	
Center Wavelength	$\lambda_c$	1295	1310	1325	nm	
Average Power at Receiver				3	dBm	
Receive reference (max)				-26	dB	
Receiver Sensitivity (OMA)	P <sub>sens</sub>	-	-	-12.0	dBm	1
Stressed receiver sensitivity (OMA)				-9.5	dBm	2
LOS De-Assert	LOS <sub>D</sub>			-12	dBm	
LOS Assert	LOS <sub>A</sub>	-30			dBm	
LOS Hysteresis		0.5			dB	

### Notes:

1. For 25G-LR with FEC, receiver sensitivity is defined at 5E-5 BER level, not 10-12 BER level.
2. Measured with conformance test signal at TP3 for BER=5E-5.

## Timing and Electrical

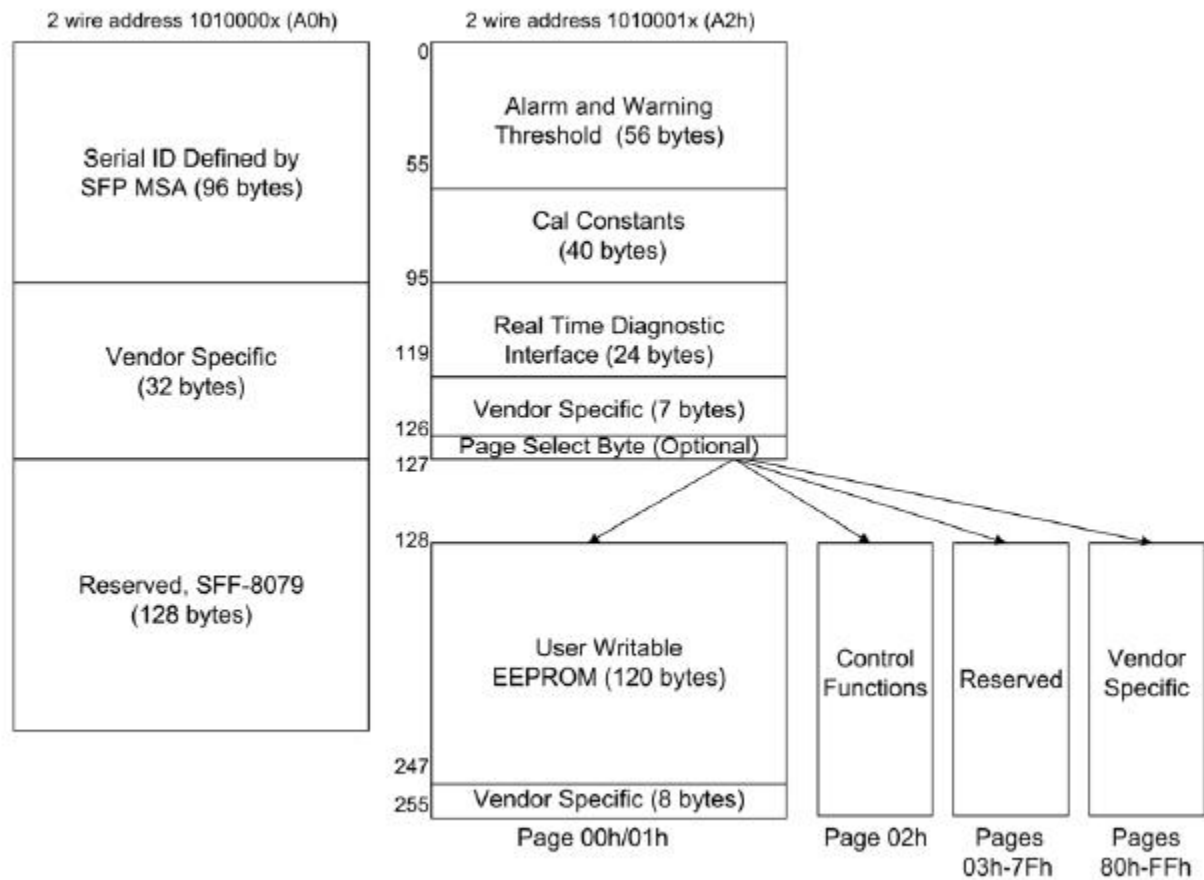
<i>Parameter</i>	<i>Symbol</i>	<i>Min.</i>	<i>Max.</i>	<i>Unit</i>	<i>Conditions</i>
Tx_Disable assert time	t_off		100	µs	Rising edge of Tx_Disable to fall of output signal below 10% of nominal
Tx_Disable negate time	t_on		2	ms	Falling edge of Tx_Disable to rise of output signal above 90% of nominal. This only applies in normal operation, not during start up or fault recovery.
Time to initialize 2-wire interface	t_2w_start_up		300	ms	From power on or hot plug after the supply meeting Table 8.
Time to initialize	t_start_up		300	ms	From power supplies meeting Table 8 or hot plug or Tx disable negated during power up, or Tx_Fault recovery, until non-cooled power level I part (or non-cooled power level II part already enabled at power level II for Tx_Fault recovery) is fully operational.
Time to initialize cooled module and time to power up a cooled module to Power Level II	t_start_up_cooled		90	s	From power supplies meeting Table 8 or hot plug, or Tx disable negated during power up or Tx_Fault recovery, until cooled power level I part (or cooled power level II part during fault recovery) is fully operational. Also, from stop bit low-to-high SDA transition enabling Power Level II until cooled module is fully operational
Time to Power Up to Level II	t_power_level2		300	ms	From stop bit low-to-high SDA transition enabling power level II until non-cooled module is fully operational
Time to Power Down from Level II	t_power_down		300	ms	From stop bit low-to-high SDA transition disabling power level II until module is within power level I requirements.
Tx_Fault assert	Tx_Fault_on		1	ms	From occurrence of fault to assertion of Tx_Fault
Tx_Fault assert for cooled module	Tx_Fault_on_cooled		50	ms	From occurrence of fault to assertion of Tx_Fault
Tx_Fault Reset	t_reset	10		µs	Time Tx_Disable must be held high to reset Tx_Fault
RS0, RS1 rate select timing for FC	t_RS0_FC, t_RS1_FC		500	µs	From assertion till stable output
RS0, RS1 rate select timing non FC	t_RS0, t_RS1		24	ms	From assertion till stable output
Rx_LOS assert delay	t_los_on		100	µs	From occurrence of loss of signal to assertion of Rx_LOS
Rx_LOS negate delay	t_los_off		100	µs	From occurrence of presence of signal to negation of Rx_LOS

## Memory Organization

The transceivers provide serial ID memory contents and diagnostic information about the present operating conditions by the 2-wire serial interface (SCL, SDA).

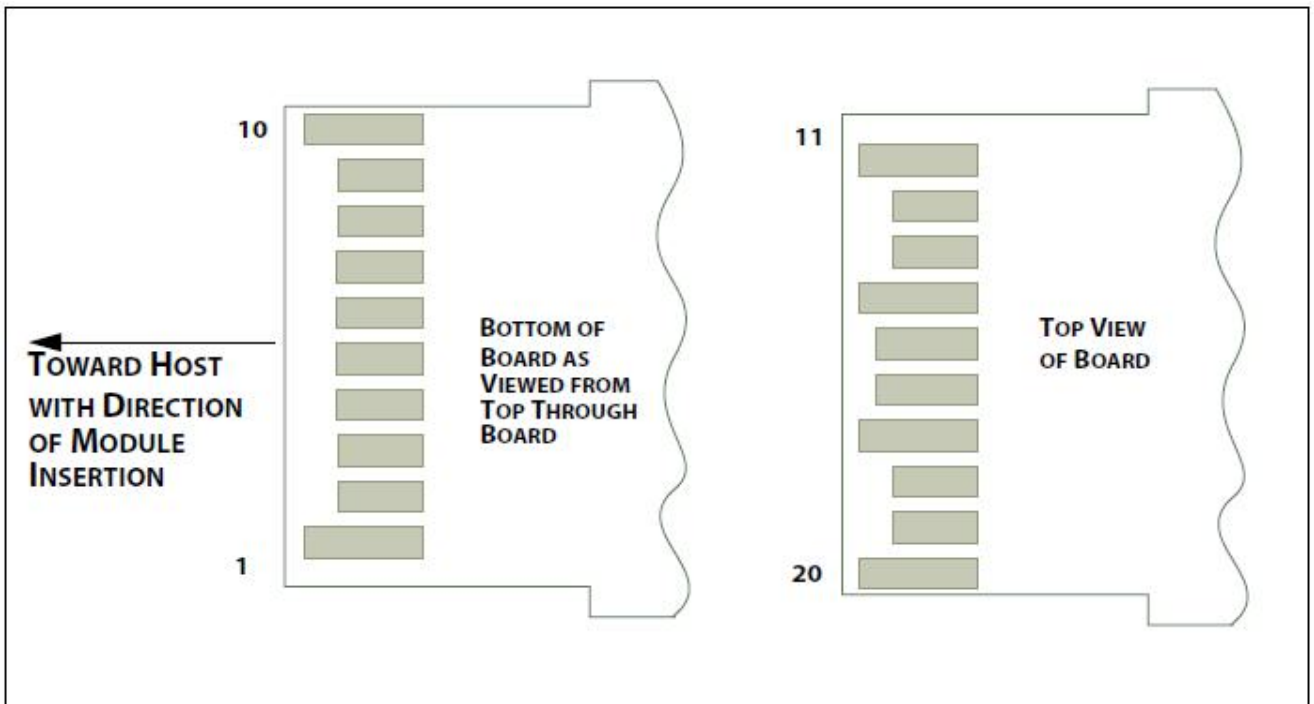
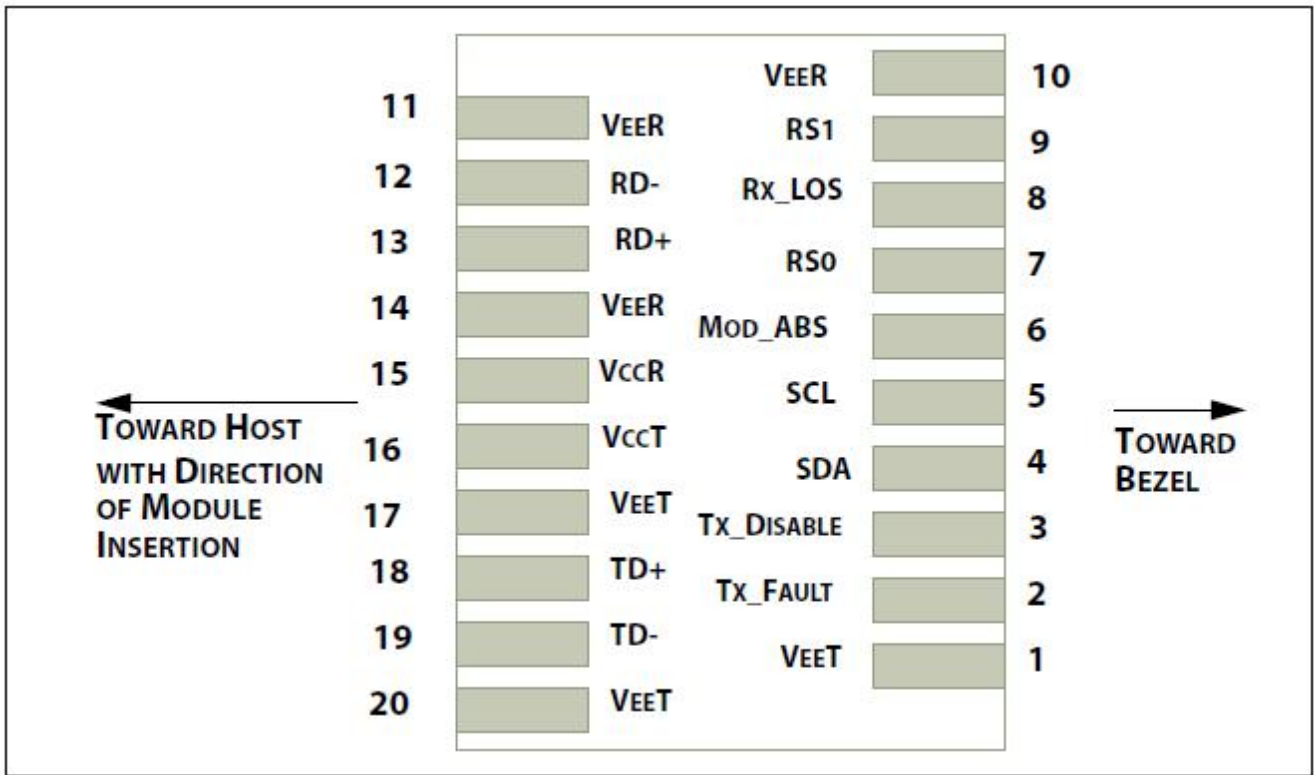
The memory map specific data field defines as following.

### Two-wire Interface Fields



### TWO-WIRE INTERFACE FIELDS

# Pin Definitions



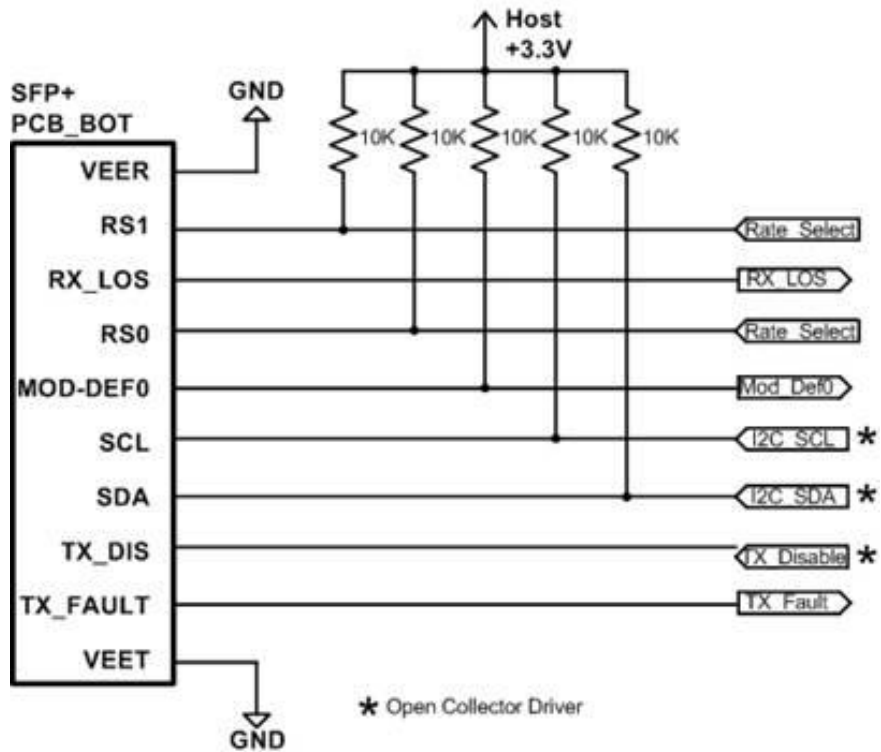
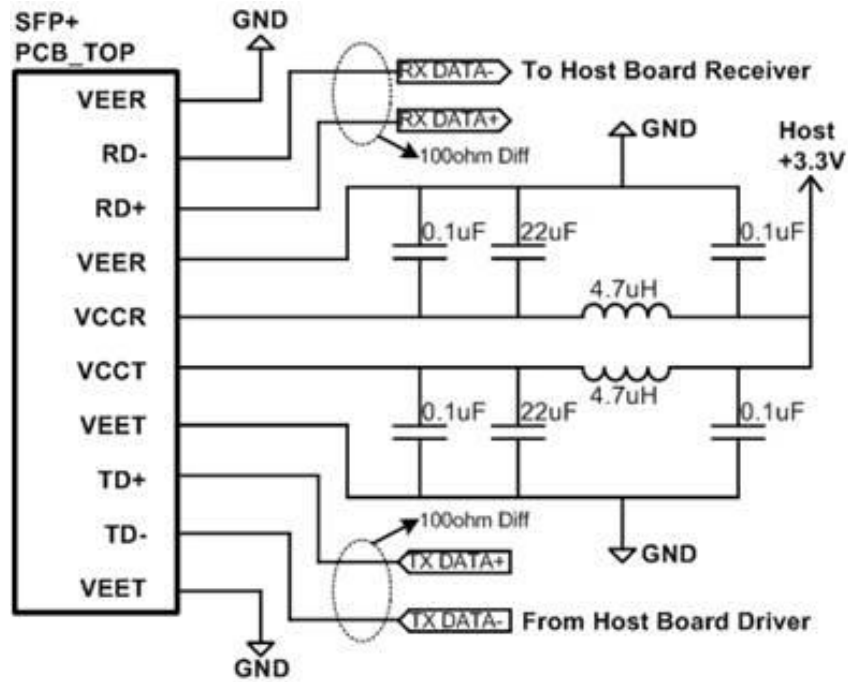
## Pin Descriptions

PIN	Logic	Symbol	Name / Description	Note
1		VeeT	Module Transmitter Ground	1
2	LVTTL-O	TX_Fault	Module Transmitter Fault	2
3	LVTTL-I	TX_Dis	Transmitter Disable; Turns off transmitter laser	
4	LVTTL-I/O	SDA	2-Wire Serial Interface Data Line	2
5	LVTTL-I	SCL	2-Wire Serial Interface Clock	2
6		MOD_ABS	Module Definition, Grounded in the module	
7	LVTTL-I	RS0	Receiver Rate Select	
8	LVTTL-O	RX_LOS	Receiver Loss of Signal Indication Active LOW	
9	LVTTL-I	RS1	Transmitter Rate Select (not used)	
10		VeeR	Module Receiver Ground	1
11		VeeR	Module Receiver Ground	1
12	CML-O	RD-	Receiver Inverted Data Output	
13	CML-O	RD+	Receiver Data Output	
14		VeeR	Module Receiver Ground	1
15		VccR	Module Receiver 3.3 V Supply	
16		VccT	Module Receiver 3.3 V Supply	
17		VeeT	Module Transmitter Ground	1
18	CML-I	TD+	Transmitter Non-Inverted Data Input	
19	CML-I	TD-	Transmitter Inverted Data Input	
20		VeeT	Module Transmitter Ground	1

### Notes:

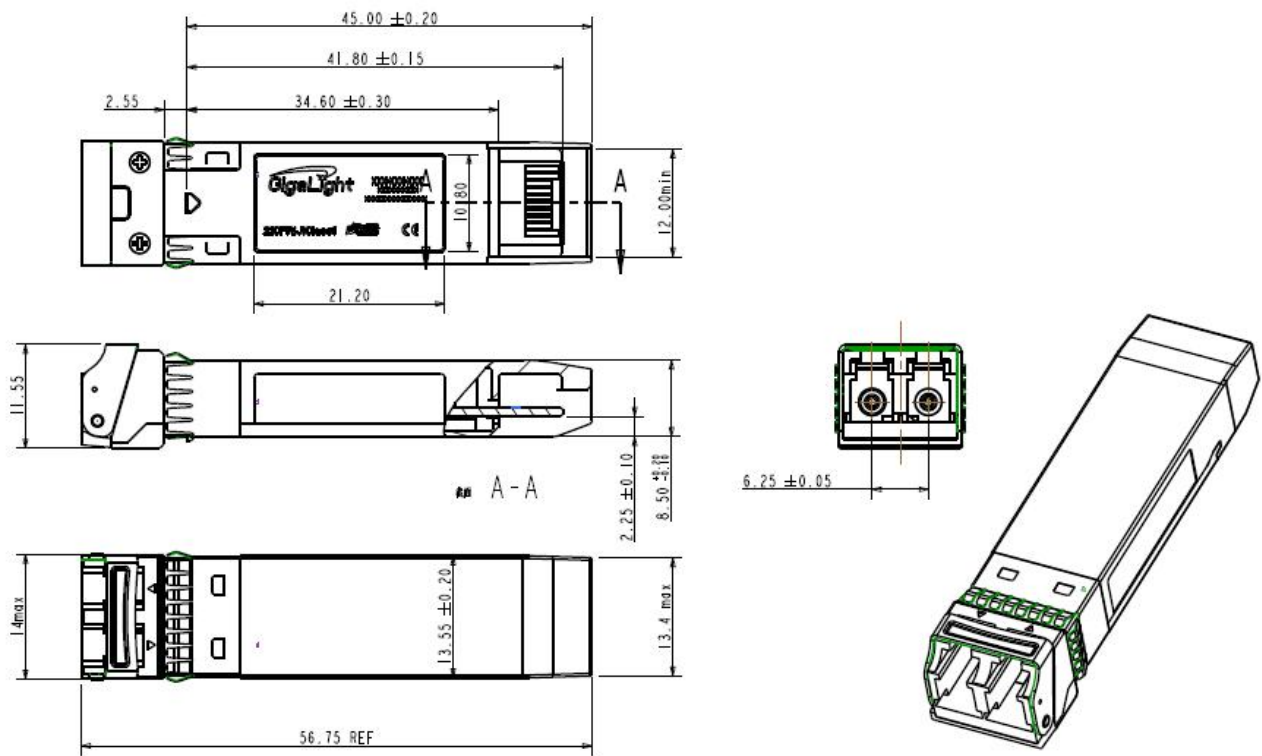
1. Module ground pins GND are isolated from the module case.
2. Shall be pulled up with 4.7K-10K ohms to a voltage between 3.15V and 3.45V on the host board.

## Recommended Interface Circuit





## Mechanical Dimensions



## Regulatory Compliance

Feature	Standard
Laser Safety	IEC 60825-1:2014 (Third Edition)
Environmental protection	2011/65/EU
CE EMC	EN55032:2015 EN55035:2017 EN61000-3-2:2014 EN61000-3-3:2013
FCC	FCC Part 15, Subpart B; ANSI C63.4-2014

## References

1. SFP28 MSA
2. Ethernet IEEE 802.3cc
3. Directive 2011/65/EU of the European Parliament and of the Council, "on the restriction of the use of certain hazardous substances in electrical and electronic equipment," July 1, 2011.